Flip-Chip Integration of 1060 nm VCSELs and Photodiodes on Polymer PICs for Out-of-Plane Coupling

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Abstract: We demonstrate flip-chip integration of 1060 nm VCSEL and photodiode arrays on polymer PICs using diced 45° facets and wafer-level coining. This approach achieves out-of-plane coupling and validated loss budgets for potential co-packaged optical interconnects. © 2026 The Author(s)

1. Introduction

Co-packaged optics (CPO) demand high-speed and energy-efficient interconnects for modern short-reach datacenter environments. Vertical-Cavity Surface-Emitting Laser (VCSEL) based links are particularly appealing for CPO due to their efficiency, scalability and manufacturing maturity [1]. However, most photonic integrated circuits (PICs) guide light in-plane, while VCSELs emit light vertically. Traditional solutions, such as silicon photonics (SiPh) gratings or silicon micromirrors, add fabrication complexity and alignment challenges [2]. In addition, wire-bonded packaging solutions further increases parasitic impedances, degrading bandwidth and reliability [3].

This work demonstrates flip-chip integration of 1060 nm single-mode VCSEL and photodiode (PD) arrays onto polymer PICs (PolyBoard), employing diced 45° facets for efficient out-of-plane light coupling. The PolyBoard platform's low refractive index contrast produces large mode field diameters compatible with VCSEL emission, eliminating the need for high-index gratings and simplifying assembly. We further developed wafer-level bumping and coining processes and validated the integration of flip-chip VCSELs and PDs experimentally by characterizing their light-current-voltage (L-I-V) and effective responsivity on the PolyBoard.

2. PolyBoard PIC Design, Facet Engineering, and Flip-Chip Integration

The PolyBoard PIC is fabricated using ZPU-Chemoptics® polymer, featuring a core refractive index of approximately 1.454 at 1060 nm and a cladding index of 1.449. This configuration minimizes propagation losses (0.4 dB/cm) while maximizing the mode field diameter (MFD). At the facet, the square waveguides (5.7 µm × 5.7 µm) are tapered linearly to a width of 6.7 µm, resulting in a MFD of 7.5 µm × 6.8 µm at the $1/e^2$ level, which aligns well with the near-circular VCSEL emission profile and offers improved coupling efficiency and coupling tolerance over high-contrast silicon photonics platforms.

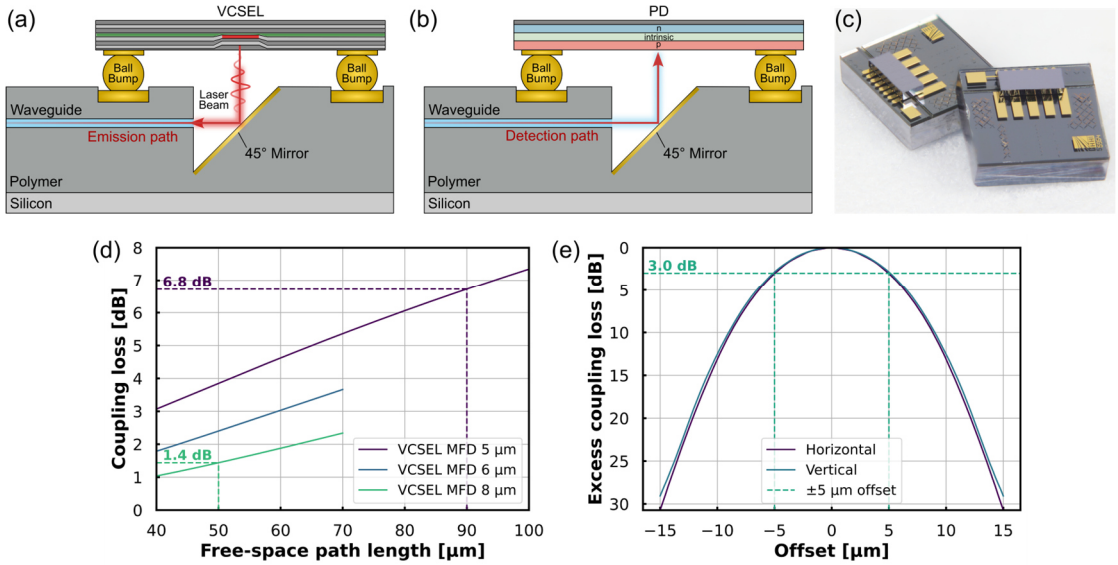

Fig. 1. Schematic of flip-chip **(a)** VCSEL and **(b)** PD on PolyBoard. **(c)** Device photo. **(d)** Simulated coupling loss versus path length for VCSELs with different MFDs. **(e)** Simulated coupling tolerance for the VCSEL with 5 µm MFD.

To enable efficient out-of-plane light routing, a 45° facet is diced through the waveguide using a fast-rotating, diamond-grain blade. This process leverages high blade rotation and slow feed rates to minimize surface roughness, while intrinsic polishing during sawing further enhances facet quality [4,5]. The facet is subsequently coated with a thin gold layer via directed evaporation to maximize reflectivity. For PD integration, a similar facet directs in-plane guided light upward to the flip-chipped PD.

The waveguide facet geometry is optimized using FIMMWAVE simulations. Single-mode VCSELs with MFDs of 8 µm, 6 µm, and 5 µm are modeled as near-Gaussian emitters based on measured near-field profiles and divergence at 1060 nm. Overlap integrals quantify coupling losses through the free-space section between VCSEL and waveguide. Simulations predict losses as low as 1.4 dB for a 50 µm free-space path with an 8 µm MFD.

Flip-chip integration utilizes an automated wafer-level ball bumping process, developed on the PolyBoard platform, achieving solder ball diameters below 40 µm and a mean bump height of 19.5 µm (RMS ±2.4 µm). Wafer-level coining further refines bump diameter to 36.0 µm and improves uniformity (RMS ±1.8 µm), reducing height to 13.2 µm with RMS ±0.9 µm, ensuring coplanarity for arrays. Visual alignment marks assist precise ultrasonic bonding, performed using the FINEPLACER® lambda 1 system, to complete the flip-chip assembly.

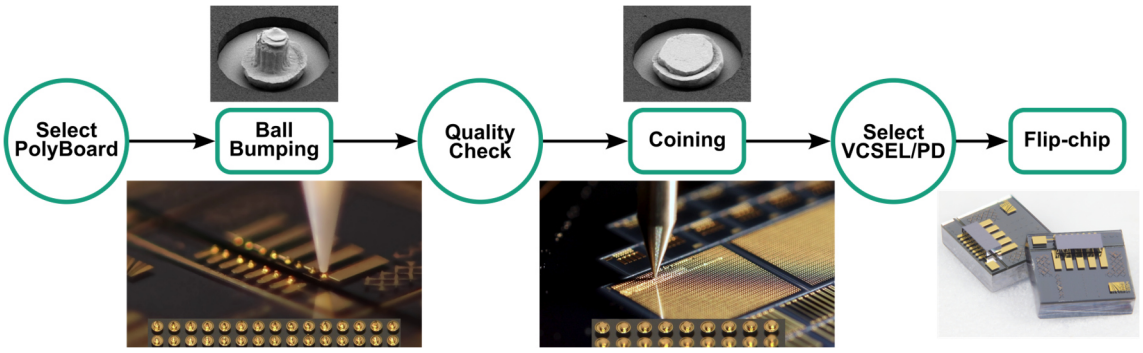

Fig. 2. Schematic illustration of the flip-chip integration process on the PolyBoard platform, including representative SEM images and detailed process views at each critical fabrication step.

3. Experimental Results and Characterization

L-I-V measurements were performed by coupling a single-mode fiber (SMF) at the output of the VCSEL-on-PolyBoard assembly. The bare VCSEL with a 5 µm MFD exhibited an output power of 6.2 dBm. For the experimental setup with a 90 µm gap, simulations showed a 6.8 dB optical loss (Fig. 1 (d)). The ultrasonic bonding process, with an alignment accuracy of ±5 µm, introduced an additional loss of approximately 3.0 dB (Fig. 1 (e)). The fiber-to-PolyBoard coupling further contributed 0.8 dB loss. The cumulative losses resulted in a measured total output power of −4.0 dBm, which is in close agreement with the expected value of −4.4 dBm based on the loss budget.

The PolyBoard-integrated PDs exhibited an average effective responsivity of 0.36 A/W, compared to 0.55 A/W for bare dies. Considering the fiber–chip coupling introduces 0.8 dB loss, a coupling loss of 1.0 dB at the PolyBoard–PD interface can be inferred.

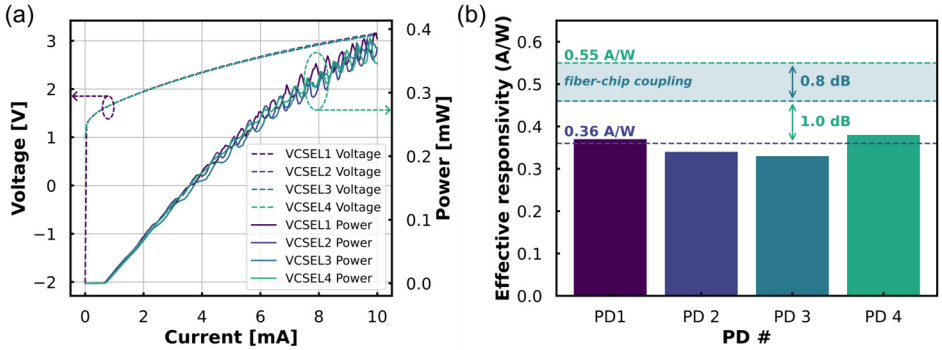

Fig. 3. **(a)** L-I-V measurement of the flip-chipped VCSELs. **(b)** Effective responsivity of the flip-chipped PDs.

4. Conclusion

We report flip-chip integration of 1060 nm single-mode VCSEL and PD array on polymer PICs with out-of-plane coupling via 45° mirror facets. Key fabrication innovations include automated wafer-level bumping and coining, achieving solder bump diameters of 36.0 µm and heights of 13.2 µm with RMS uniformity as low as ±0.9 µm. Experimental measurements closely match simulated results, confirming cumulative optical losses of 6.8 dB across the free-space gap, approximately 3 dB from bonding, and 0.8 dB due to fiber coupling. The PolyBoard-PD interface achieves efficient optical coupling with losses as low as 1.0 dB.

Acknowledgements

The authors acknowledge support from the Horizon Europe project SPRINTER (Grant Agreement ID: 101070581) and NVIDIA.

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