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Folded electro-optical modulators operating at CMOS voltage level in a thin-film lithium niobate foundry process

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Abstract: Integrated electro-optical modulators with small footprints and low half-wave voltage are essential for applications requiring high integration density and low power consumption. Modulators based on thin-film lithium niobate technology have been proven to perform excellently, both in terms of low voltage and high bandwidth operation. However, achieving half-wave voltages of ∼1 V, which allows to directly drive the modulator with CMOS circuits, typically requires long structures. Folding the device is a possible approach to achieve a CMOS-compatible voltage level in a compact design. Yet, this method requires meticulous design and advanced manufacturing technology. To achieve large scale deployment of this technology, it is imperative to further develop thin-film lithium niobate photonic integrated circuits manufacturing. Here, we address these requirements and report folded electro-optical modulators, operating at 1550 nm in TE polarization, with half-wave voltage as low as 0.9 V or bandwidths up to beyond 40 GHz in a compact 5 mm × 5 mm chip fabricated in CSEM's open-access foundry process using standardized process design kit components.

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1. Introduction

Due to the exponential growth in internet traffic driven by video streaming, cloud services, and the demand for AI tools, optical telecommunication's infrastructure face unprecedented pressure to handle the required load [1,2]. Photonic Integrated Circuits (PICs) have emerged as a promising technology to manage these issues, serving both short and long-haul applications. Electro-Optical (EO) modulators, enabling precise and rapid modulation of optical signal, are key elements of PICs and play a significant role in optical communication links [1–4]. Besides telecom and datacom, integrated EO modulators find applications in LiDAR systems, optical coherence tomography, sensing, and quantum photonics [5–9], to name a few. So far, silicon photonics has been the technology of choice for integrated modulators in datacom, due to its large-scale availability given by complementary metal–oxide–semiconductor (CMOS) foundries. Silicon, however, lacks Pockels effect, which is paramount for high quality and efficient EO modulation. Several alternative modulation schemes based on plasma dispersion have been proposed [10–12]. While a half-wave voltage below 1 V has been demonstrated [13], nonlinearity of free-carrier dispersion, high optical losses, and dopant diffusion at high temperature [14], impose limitations on the overall performance achievable through the doping approach. Thermo-optical [15] and micro-electro-mechanical systems (MEMS) [16] modulators have also been extensively investigated, but the inherently slower thermal response of most materials and the mechanical movement of microstructures severely limit their bandwidth to ∼100 kHz and ∼10 MHz respectively. Moreover, the relatively high power consumption (a few mW for π phase shift) of thermal modulators remains a significant bottleneck for scaling up PICs based on these

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components. Thermal cross-talk is also an important limit for quantum applications, especially if cryogenic temperatures are required. MEMS offer compact solutions for modulations, but are prone to failures such as electrostatic pull-in and not fully developed in any standard platform yet. In this context, the recent development of Thin-Film Lithium Niobate on Insulator (TFLN) technology represents a breakthrough. TFLN combines a wide transparency window extending from 350 to 5550 nm [17], propagation losses typically below 0.3 dB/cm and as low as 0.027 dB/cm [17,18], and a relatively large EO coefficient ($r_{33} = 30.8$ pm/V) [17], making it an excellent choice for creating fast and power-efficient optical modulators. In addition, unlike Si modulators, EO modulation in TFLN does not suffer from spurious amplitude variations. Modulators with bandwidths exceeding 100 GHz [19–29] and half-wave voltages of 1 V and less [28,30,31] have been demonstrated in TFLN. However, the fabrication technology for TFLN PICs has not yet reached the maturity required to fully meet the demand for a reliable device performance and high yield production. This presents a significant challenge for photonic designers looking to utilize this technology. There is an urgent need for the development of an open-access, standardized TFLN PIC platform that offers manufacturing technologies to designers. Such a platform would be supported by Process Design Kits (PDKs), containing rigorously validated building blocks that adhere to specific design rules, ensuring a reliable and consistent fabrication process [32,33]. By enabling the development of more efficient and compact PICs, TFLN technology is poised to significantly impact the future of telecommunications, data centers, and various other applications where speed, power efficiency and compactness are paramount.

The superior EO properties of TFLN enable not only high-speed modulation, but also low voltage operation. Operating voltages below 1 Volt allow for the direct driving of the modulators using integrated CMOS circuitry, which reduces the overall power consumption, simplifies systems' architecture, contributes to reduced latency, and enhances the reliability of devices while leading to a reduced unit cost [21]. Another notable benefit of TFLN modulators in comparison with the bulk versions is their potential to significantly reduce the device size, which is critical for a wide range of applications, as limited space is often a concern. Typical values of voltage-length product of TFLN modulators are around 2-3 V.cm, demonstrated in recent works [34]. To reach a half-wave voltage at the 1 V level while maintaining the design compact, folded modulators have been proposed [30,35–37].

Here, we report folded TFLN EO Mach-Zehnder Modulators (MZMs) that show comparable capabilities to those demonstrated in literature. The modulators are designed by fully relying on our PDK components following design rules and fabricated using our standard foundry process. Our technology stack also features a dual-layer metallization structure that enables complex radio frequency routing process and back-end-of-line integration. We elaborate on our recent demonstration with design methodology and extensive experimental results and discussion [33]. These results highlight capability of our open-access foundry to provide large-scale, high-performance TFLN PICs to address the industrial growing demand.

2. Folded modulators design

In EO MZMs, the Pockels effect is harnessed to change the phase of the optical signals travelling in the two arms of the interferometer by applying a voltage V. Assuming that the input optical power is equally split in the two arms, the intensity at the output of the interferometer I_o is related to the intensity at the input I_i by $I_o = \frac{1}{2}I_i + \frac{1}{2}I_i \cos\varphi = I_i\left[\cos\left(\frac{\varphi}{2}\right)\right]^2$, where φ is the phase difference between the signals travelling in the two arms. In a push-pull configuration, in which opposite voltages $+V$ and $-V$ are applied to the two arms, the phase difference is given by $\varphi = \varphi_1 - \varphi_2 = \pi\frac{V}{V_\pi} - \pi\frac{-V}{V_\pi} = 2\pi\frac{V}{V_\pi}$, where V_π is the voltage required to have a π phase shift. The transmittance of the device is therefore given by $T = \frac{I_o}{I_i} = \left[\cos\left(\pi\frac{V}{V_\pi}\right)\right]^2$ and it is thus possible to control the transmitted optical power by controlling the applied voltage. A common approach to reduce the operating voltage of an EO modulator is to increase its length. However, this strategy has trade-offs, including increased chip size. To address the challenge of accommodating a lengthy EO device within limited space, folding techniques are often employed. In the case of x/y cut TFLN, however, the electric field direction would be inverted upon folding if electrodes are not carefully placed, therefore cancelling out the accumulation of the phase change in the Mach-Zehnder interferometer (MZI). Poling the folded waveguide or employing interdigitated T-rails electrodes have been shown to be two techniques to solve this problem [35,38]. However, achieving uniform poling across the entire length of the waveguide and precise electrodes placement can be challenging. Alternatively, crossing the two arms of the MZI can avoid the electric field flipping [30,39]. In our design we adopted this option, which involves strategically using waveguide crossings and incorporating two levels of metallization layers to ensure efficient operation. Additionally, for high-speed applications, a meticulous design approach is essential to meet the criteria for a traveling wave modulator and achieve necessary impedance matching. The high-speed performances of an EO modulator are indeed limited by (1) RF losses, which could significantly decrease the intensity of the modulating signal, (2) difference between the phase velocity of the RF signal and the optical group velocity, which may result in inefficient modulation due to the electrical signal not being continuously applied to the optical pulse, and (3) mismatch between the impedance of the transmission line and the impedance of external electronics, which could result in unwanted power reflection.

Figure 1(a) illustrates the layout of our folded MZI modulator, showcasing our technology layers. The circuit incorporates several optimized building blocks from the PDK, including MMI (Multi-Mode Interference) beam splitters [29], waveguide crossings, and edge couplers. Within this design, the optical arms and electrodes undergo multiple 180° turns, effectively increasing the signal path length while maintaining a compact form, at the cost of increased device width. To minimize the half-wave voltage, we employ a push-pull electrode configuration. Notably, attempting to implement an on-chip folded modulator architecture without two levels of metallization would pose significant challenges and result in inefficiencies related to modulator actuation (higher drive voltage) and optical loss. Alternatively, a similar architecture could be realized using a single metal layer, with additional back-end-of-line processing to establish necessary electrical connections. However, it’s important to emphasize that the push-pull configuration necessitates waveguide crossings at the U-turns, and the presence of two metallization levels connected via vias is crucial to prevent waveguide coverage by metallization, which would lead to substantial optical losses. In our design, light is guided in 0.8 µm wide waveguides. The simulated optical mode at 1550 nm wavelength and TE polarization is shown in the center-left panel of Fig. 1(b). The signal is split into the two arms of a MZM by a 50/50 2×1 MMI with dimensions shown in the left panel of Fig. 1(b). A waveguide crossing (right panel of Fig. 1(b)) with simulated crosstalk <0.01 dB is used at each waveguide turn. A signal gap of 13.7 µm and a signal width of 4.5 µm were chosen to ensure 50 Ω impedance matching with the standard measurement tools (mismatch <1 Ω between 10-50 GHz, see Fig. 1(c)), allowing to minimize RF signal reflections, and velocity matching between the RF and optical fields to deliver efficient EO response, ensuring efficient modulation along the entire modulator length (Fig. 1(d)). The calculated RF field is shown in the center-right panel of Fig. 1(b). The signal gap and signal width were intentionally chosen to be slightly larger than the ones that would give perfect velocity matching. This was done to decrease the RF losses, which below 50 GHz are a greater limiting factor of the modulator bandwidth than the velocity mismatch if the latter is limited to $n_{g,\ opt} - n_{eff,\ RF} < 0.1$, where $n_{g,\ opt}$ and $n_{eff,\ RF}$ are the optical group and RF effective indexes respectively [17].

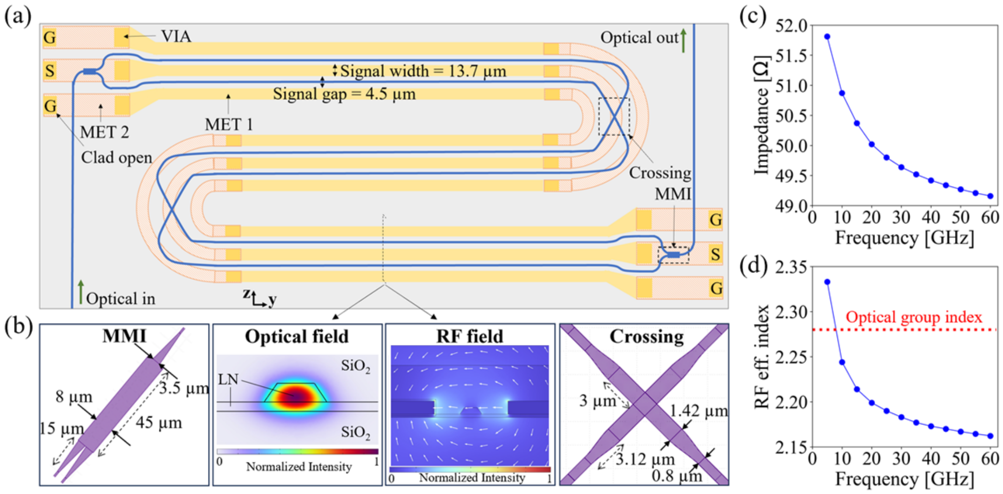

Fig. 1. (a) Schematic top view of the chip. (b) Schematic view of the MMI (left box), simulated optical field at 1550 nm wavelength in TE polarization (center-left box), simulated RF field at 50 GHz frequency (center-right box, the arrows show the electric field direction), and schematic of the waveguide crossing (right box). (c) Simulated characteristic impedance of the modulators. (d) Simulated optical group index and RF effective index.

3. Fabrication

The devices are fabricated in a 150 mm wafer scale standard foundry process at CSEM. Our fabrication technology is based on commercially available thin-film lithium niobate on insulator wafers which consist of a stack with 600 nm thick mono-crystal x-cut $\mathrm{LiNbO_3}$ layer on top of a 4.7 μm buried thermal oxide (BOX) layer. Waveguides are patterned by etching 400 nm of $\mathrm{LiNbO_3}$ by an optimized ion milling technology. All layers are protected by a silicon oxide cladding. Then, a specialized process module referred to as “clad open”, is incorporated to provide designers the option to selectively remove the cladding. This feature allows for specific applications, such as creating access points to the metal pads or directly interfacing with the waveguides. The final chip release process yields to smooth facets which are crucial for achieving efficient light coupling at both the input and output interfaces of the device. Several modulators were fabricated in the standard process, and here we present the measurements for modulators with signal lengths ranging from 0.99 cm to 2.97 cm were fabricated and characterized.

4. Results and discussion

4.1. Experimental setup

The comprehensive performance evaluation of the modulator focuses on two primary domains: DC (Direct Current) for assessing the modulation efficiency $V_\pi L$, and RF (Radio Frequency) measurements to investigate overall modulator performance. In DC measurements, the half-wave voltage, insertion loss, and extinction ratio are measured. Within the RF measurements, two key aspects are considered: Electrical-Electrical (EE) measurements, which evaluate electrical losses and design quality in terms of impedance matching and microwave phase index, and Electro-Optical (EO) measurements, which are bounded by EE performance, but they are also sensitive to velocity mismatch, and they assess modulator performance at high frequencies. Figure 2(c) illustrates the characterization setups used for DC measurements and RF measurements of the chip, which is shown in Fig. 2(a) and Fig. 2(b). Light from a mode-hop-free laser emitting at 1550 nm (Toptica, CTL 1550) is directed to the chip through a polarization controller (which selects TE polarization) and a lensed polarization maintaining fiber. Edge couplers designed to efficiently couple 1550 nm light and 6 degrees of freedom coupling stages, with piezoelectric actuators controlled by a home-made software, are used to maximize the coupled power. To determine the DC half-wave voltage (Vπ) of the modulators, a low-frequency characterization is performed. A triangular electrical signal with a frequency of 5 kHz is directly applied to the electrodes, and the resulting modulated optical output is recorded by an InGaAs photodetector (Thorlabs, PDA20CS2). The photodetector's response is acquired using a 500 MHz bandwidth oscilloscope (Keysight, MXR054A). RF electrical measurements consist in applying, via ground-signal-ground electrical probes (FormFactor, 50 GHz Z probes), a signal of variable frequency, from 100 MHz to 50 GHz, generated by a Virtual Network Analyzer (Rohde&Schwarz ZNA) to one end of the modulator and recording the transmitted and reflected signal with the same VNA. The system is calibrated using a calibration substrate (Cascade Microtech, CSR-8). In RF EO measurements, a DC bias, delivered by a bias tee (Anritsu, V255), is applied to drive the modulators at the quadrature point. The microwave signal generated by the VNA is applied to the electrodes, and the optical output is recorded by a fast photodetector (Thorlabs, DX50AF) and sent to the output port of the VNA. A 50 Ω termination is applied to the output-end of the electrodes to ensure impedance matching. The system is calibrated at the cables level using a calibration kit (Agilent, 85056D), whereas the RF responses of the probes and of the photodetector are de-embedded in data analysis.

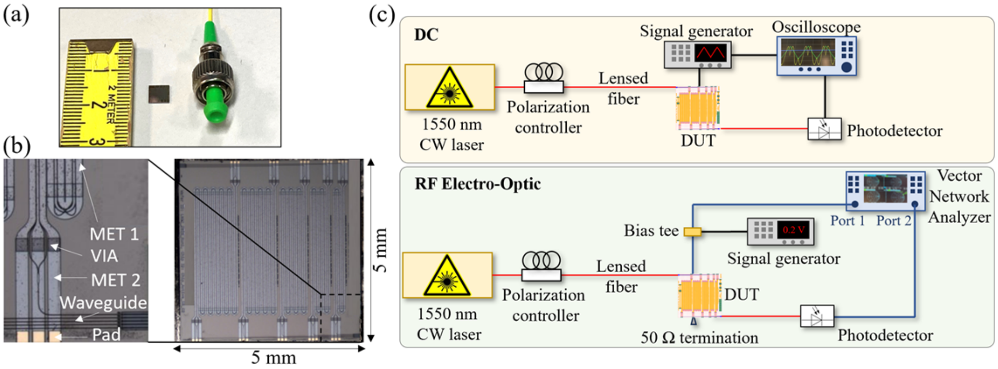

Fig. 2. (a) Photograph of the chip. (b) Optical micrographs of the device under test. (c) Schematic of the experimental setup for DC (top) and RF electro-optic (bottom) measurements.

4.2. *Folded modulators characterization*

Figure 3 shows the modulated optical response of the modulators as a function of the applied bias voltage. The half-wave voltage ranges from 2.5 V for the shorter modulator, to 0.9 V for the longer one, corresponding to an efficiency V_π.L (L being the length of the modulator) of 2.5-2.7 V.cm. As expected, V_π decreases with the length, highlighting the importance of the folded design to achieve V_π at the 1 V level in a compact chip. For the longer modulator, the half-wave voltage value falls withing the CMOS-level-voltage operation that brings a substantial advantage for the EO modulator enabling to drive the device with fully integrated CMOS electrical circuits, without the need of off-chip amplification. Thanks to our folded modulator design, we achieved such value in a compact 5 mm × 5 mm chip. The total device insertion losses are between 12 and 14 dB, slightly increasing for longer modulators, but mainly driven by fiber-to-chip and chip-to-fiber coupling losses (ca 4 dB/facet) and losses in the MMIs. The extinction ratio is relatively high, above 17 dB for all modulators (see Fig. 3, insets).

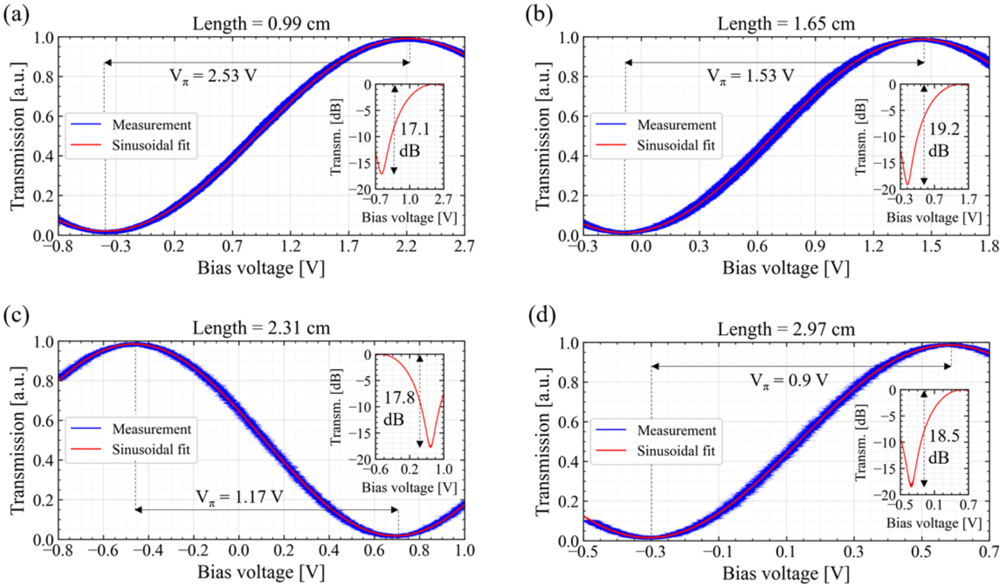

Fig. 3. Measured (blue) and fitted (red) DC electro-optical response of modulators with length of 0.99 cm (a), 1.65 cm (b), 2.31 cm (c), and 2.97 cm. The insets show the transmission in dB scale.

The measured EE response is reported in Fig. 4, with Fig. 4(a) and Fig. 4(b) showing the S_{11} and S_{21} parameters respectively. The reflection below 20 dB (Fig. 4(a)) confirms the validity of our design in terms of impedance matching, as confirmed by the RF characteristic impedance, extracted from the EE measurements, shown in Fig. 5(b). The measured mismatch between the RF effective index and the optical carrier group index is <0.2 at 50 GHz (see Fig. 5(c)), higher than the simulated one (Fig. 1(d)), that could be attributed to fabrication inaccuracies. At this level of velocity-mismatch, a theoretical limit of 95 GHz bandwidth would be reached for a length of 0.99 cm, according to the formula $\Delta f = 2c/\pi l \Delta n$ [40], where c is the speed of light, l the modulator length, and Δn the difference between the RF effective index and the optical group index. This value is considerably higher than the 26 GHz EE bandwidth experimentally observed (see Fig. 4(b), blue curve). We therefore identify the RF losses of 2-12 dB/cm in the 0.1-50 GHz range (see Fig. 5(a)) as the bandwidth limiting factor. The electrical loss for a modulator of length L can be modelled as $A + \left(a_c\sqrt{f} + a_d f\right) L$, where f is the frequency, A the DC loss due to impedance mismatch, a_c and a_d are factor related to the conductor and dielectric loss respectively. By fitting the measured loss to this equation (Fig. 5(a) inset), we estimate $A = 2.63$ dB, $a_c = 0.45$ dBcm^{-1}GHz$^{-1/2}$, and negligible a_d. This indicates that the main loss mechanism is conductor loss, consistent with previous observation for frequencies below 50 GHz [41,42]. An investigation of the origin of the conductor loss is ongoing.

Figure 6 shows the RF EO response of the modulators. A 3 dB bandwidth higher than 46 GHz and of 20 GHz is achieved in the shortest and longest modulators respectively. The bandwidth is measured with respect to a low frequency reference of 3 GHz (see Fig. 6(b)). The slope of the EO S_{21} is well reproduced by simulations (dashed curves in Fig. 6), which however fail to capture the drop of the response at frequencies below 3 GHz. We hypothesize it relates to improper impedance capture from the simulation and/or unoptimized MET2 to MET1 transition for low frequencies. More advanced designs, like slotted electrodes, a better velocity mismatch, and improvement in the fabrication process to reduce RF losses could help in enhancing the efficiency

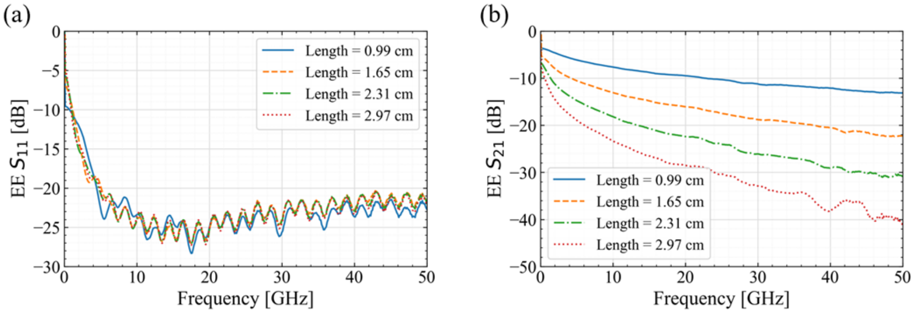

Fig. 4. Measured S_{11} (a) and S_{21} (b) electrical-electrical response for modulators of different length.

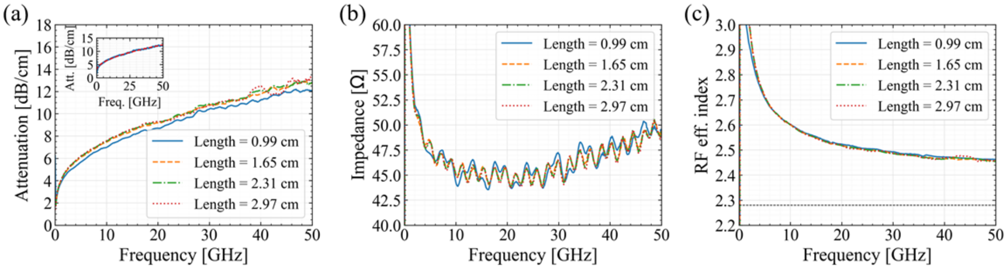

Fig. 5. Measured attenuation (a), characteristic impedance (b), and microwave effective index (c) for modulators of different length. The inset in panel (a) shows the measured attenuation for 0.99 cm length (blue curve) and the fit to the equation $A + \left(a_c\sqrt{f} + a_d f\right) L$ (red dashed curve).

in terms of the operating voltage and the bandwidth. Table 1 summarizes the modulators' performances. Despite the potential improvements in the design and RF losses, the performances of our modulators are already on par with the state-of-the-art for TFLN folded modulators. For instance, Nelan et al. adopted a design with waveguide crossing similar to the one of this work and reported a half-wave voltage of 4 V and a 3 dB bandwidth of 37.5 GHz in a hybrid SiN TFLN modulator with effective interaction length of 10 mm [39]. Chen et al. harnessed a similar folded design, but with under-etching of the TFLN structure and the use of capacitively-loaded travelling-wave electrodes, to achieve 0.7 V half-wave voltage and 45 GHz EO bandwidth, at the cost of increased fabrication complexity [30]. Hu et al. demonstrated 2.74 V half-wave voltage and 55 GHz bandwidth in a modulator, based on a poled structure, of 10 mm effective length [38]. However, as we aim to large-scale fabrication, using poling instead of waveguide crossing would not be ideal in our case, as wafer-scale poling is not fully developed yet. T-rails electrodes have been used by Liu et al. to demonstrate 1.08 V half-wave voltage and 43 GHz bandwidth in 2.1 mm effective length modulator [35]. Advanced electrode designs, such as slotted electrodes, can further enhance performance while remaining within the design rules of our platform. Additional optimization, such as improved RF-optical signal velocity matching, can also contribute to further advancements.

4.3. *Wafer-scale statistical analysis*

The reliability of the library building blocks lies at the core of a foundry business. To ensure and maintain this reliability, each manufacturing run includes monitoring standard chips containing PDK components. This allows us to evaluate the reliability level and continuously improve

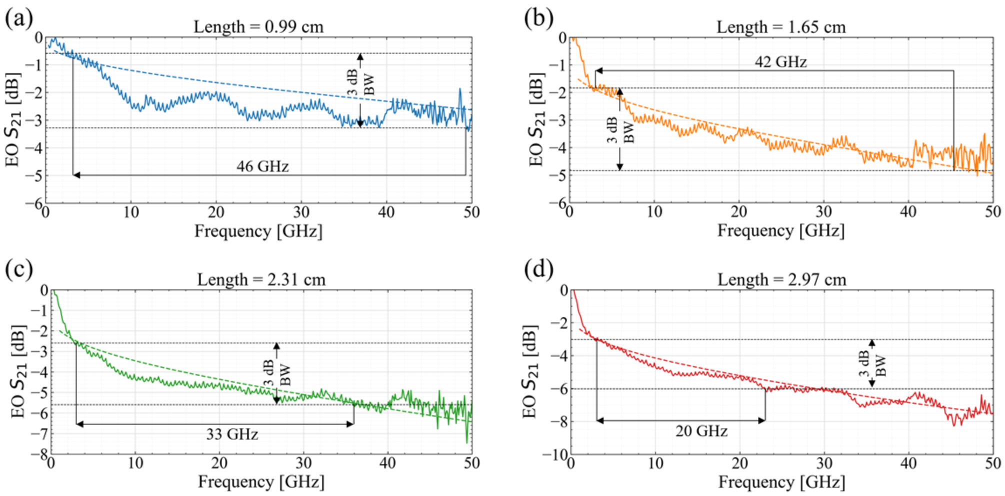

Fig. 6. Simulated (dashed curves) and measured (full curves) EO response of the (a) 0.99 cm, (b) 1.65 cm, (c) 2.31 cm, and (d) 2.97 cm long modulators.

Table 1. Summary of the modulators' performances and comparison with literature.

	Length [cm]	V_π [V]	$V_\pi L$ [V.cm]	Extinction ratio [dB]	Insertion loss [dB]	3 dB EO bandwidth [GHz]	Manufacturing platform
Our work	0.99	2.53	2.50	17.1	12.4	46 (ref. 3 GHz)	150 mm wafer foundry, standard PDK
	1.65	1.53	2.52	19.2	11.9	42 (ref. 3 GHz)	
	2.31	1.17	2.70	17.8	12.4	33 (ref. 3 GHz)	
	2.97	0.9	2.67	18.5	13.6	20 (ref. 3 GHz)	
Ref. [30]	3.3	0.7	2.31	25	14	45 (ref. NA)	Academic fab
Ref. [36]	2.1	1.08	2.27	16	14	43 (ref. 2 GHz)	Academic fab
Ref. [38]	1	2.74	2.74	NA	26.5	55 (ref. < 1 GHz)	Academic fab
Ref. [39]	1	4	4	23	21	37.5 (ref. 1 GHz)	Academic fab

the PDK. The performance and reliability of these PDK components directly influence the performance of other non-library components (such as folded modulators) that adhere to the design rules. To demonstrate the reproducibility of our foundry process and the performance consistency of our devices, we characterized two straight modulators (on the same chips), with lengths of 3.5 and 8.5 mm, from 11 chips placed at different locations on the wafer (Fig. 7(a)) and compared the statistical performances of three different wafers. For both V_π.L (Fig. 7(b)) and the EO S_{21} attenuation (Fig. 7(c)) we observed consistent inter-wafer and intra-wafer performances. In all the wafers the average V_π.L is around 2 V.cm, with a maximum range from the first to the third quartile of 0.5 V.cm for wafer 1. The RF performances of the two modulators are also consistent in different chips and wafers. The EO S_{21} attenuation at 50 GHz shows a maximum interquartile range of around 1 dB for the longer modulator in wafer 1, and an average attenuation comprised between 2.3 -2.8 dB and 2.8-3.1 dB for the short and long modulators respectively. A limited number of outliers is observed for both V_π.L and EO S_{21} attenuation. This shows the reliability of our foundry process.

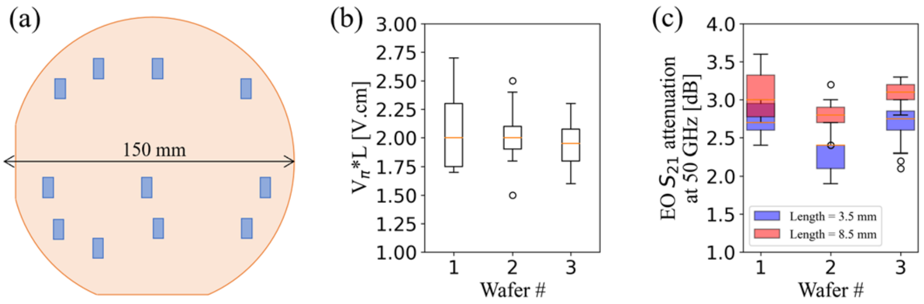

Fig. 7. (a) Location of different chips on the wafer for a statistical analysis of the modulators' performances. Boxplots of V_π.L (b) and EO S_{21} attenuation at 50 GHz (c) measured in different chips and wafers.

5. Conclusion

We presented the design, fabrication, and characterization of folded MZMs, manufactured in a TFLN PICs foundry process. The modulators, working at 1550 nm, show half-wave voltage down to below 1 V and bandwidths between from 20 to 46 GHz, all within a compact design. This suggests the potential for integrating many devices on a small chip area. Such low-power EO circuits could seamlessly interface with CMOS electrical circuits, making them suitable for applications requiring compact, power-efficient devices. The use of two metal layers greatly simplifies the design of intricate PIC components within the TFLN PIC platform. Furthermore, availability of multi-level metallization technology in a standardized PIC platform promises for facile electrical interfacing of the TFLN PICs for standard packaging approaches. Even though the performances of our modulators are already on par with other demonstrations in literature, we envision further improvements by optimization of the fabrication procedure for reduced RF losses and by an improved velocity matching of the electric and optical fields. These results showcase the progress of our foundry towards delivering large-scale, high-performance TFLN PICs in response to the market's increasing demand.

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Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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